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Scalable, flexible and high resolution patterning of CVD graphene†

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The unique properties of graphene make it a promising material for interconnects in flexible and transparent electronics. To increase the commercial impact of graphene in those applications, a scalable and economical method for producing graphene patterns is required. The direct synthesis of graphene from an area-selectively passivated catalyst substrate can generate patterned graphene of high quality. We here present a solution-based method for producing patterned passivation layers. Various deposition methods such as ink-jet deposition and microcontact printing were explored, that can satisfy application demands for low cost, high resolution and scalable production of patterned graphene. The demonstrated high quality and nanometer precision of grown graphene establishes the potential of this synthesis approach for future commercial applications of graphene. Finally, the ability to transfer high resolution graphene patterns onto complex three-dimensional surfaces affords the vision of graphene-based interconnects in novel electronics.

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Introduction

Graphene, a mono-atomic sheet of graphite, represents a new class of two-dimensional materials with properties that enable a variety of novel applications. Market predictions emphasize the use of graphene in electrode applications as the application with the largest immediate commercial impact.[1] Strong competition from mature technologies, lower performance than traditional transparent conducting oxides, and requirements on processing infrastructure put the success of graphene as large scale electrodes for solar cells or traditional displays in question.[2,3]

Graphene's high electrical conductivity considering its atomic thickness, mechanical strength, and its ability to conform to structured surfaces, however, suggest the material's potential as interconnects, in novel application such as flexible circuits,[4] wearable electronics[5] or novel displays.[6]

Competition from 1D conductors, such as nanowires and nanotubes, on the other hand, mean that additional advantages for use of graphene have to be identified, to improve the commercial appeal of this material. One such advantage is the ability to pattern graphene to expose non-conductive regions that can be used to define interconnects, transistor channels, or device terminals. High quality graphene devices with sub-micrometer resolution are routinely fabricated – a feat that is very challenging for films of 1D conductors.[7]

Common graphene patterning techniques, however, cannot exploit this inherent advantage of 2D materials in practical applications. Currently the fabrication of graphene patterns involves processes that can be categorized as mask lithography,[8] transfer printing[9] or direct patterning[10,11] of graphene after it has been transferred to the target substrate. These methods suffer from a variety of disadvantages such as lacking scalability, constraints on the target substrate or fabrication speed. Furthermore, methods to pattern the catalyst before growth have only yielded low resolution features.[12]

Several groups[13–15] including our own, have recently devised methods to directly synthesize patterned graphene by barrier guided chemical vapor deposition (CVD) growth. The methods rely on the passivation of defined areas of catalyst material and the subsequent selective growth of graphene in the unpassivated regions (Fig. 1). This approach is expected to be compatible with a wide selection of two-dimensional materials synthesized by surface-catalytic CVD processes, such as BN[16] or MoS_2.

The demonstrated ability of barrier guided CVD to generate high quality graphene on pre-patterned substrates opens up the possibility to efficiently produce novel interconnects for use in wearable or flexible electronics.

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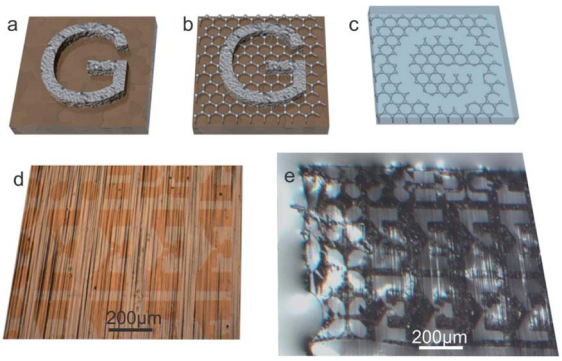

Fig. 1 (a–c) Representation of the procedure that results in patterned graphene (a) deposition of a passivation layer, (b) area-selective growth of graphene, (c) after removal of growth substrate (d) optical micrograph of copper foil after deposition of Al_2O_3-passivated patterns, (e) darkfield micrograph of resulting patterned graphene after Cu-removal (sample is floating on water during transfer, supported by a polymer membrane).

Despite these advantages, there are obstacles of the barrier guided growth of graphene patterns for use in those applications. Currently, photolithography is employed to deposit barriers which is too cost and labor intensive to be considered outside of prototype fabrication. Especially wearable and flexible electronics have requirements that are different from traditional electronic devices. A significantly larger amount of interconnects will be needed to connect distributed semiconductor segments that represent the active electronic components. Therefore, the economical and scalable production of those novel interconnects is of increased significance.

We here present a new approach to form the passivation layer on a catalyst material which is compatible with a wide variety of deposition techniques. This method can satisfy demands for low cost, large scale and high resolution and can improve the practical applicability of graphene in electronic interconnects.

Methods

Graphene was synthesized by chemical vapor deposition as previously reported[17] using copper as the catalyst material. Briefly, under low pressure (400 mTorr) a piece of copper foil (Alfa 13382) was annealed in hydrogen at 1000 °C for 30 minutes before methane gas was introduced to initiate the graphene growth. After 60 minute growth duration, the substrate was cooled down under a flow of hydrogen. Thus grown graphene was transferred onto substrates following a previously reported procedure.[12] (More information on the patterning procedures are given in the ESI.†)

Results

We chose a solution-based approach to deposit the passivation layer because of its low cost and compatibility with scalable deposition methods. We here employ an aluminum salt ($AlCl_3$) as the precursor for the passivation layer. In contact with ambient humidity and air, the deposited material forms an aluminum hydroxide and under subsequent heating forms aluminum oxide which acts as the passivation layer. This method is not only significantly easier than previous sputtering and thermal evaporation procedures, it is also compatible with a wide variety of deposition processes that are comprehensive in scale and resolution, which is demonstrated subsequently.

To accommodate demands for large area pattern generation, low cost, and production scalability, we used ink jet deposition of the passivation layer in a first set of experiments. This process is based on the area selective deposition of liquid droplets and requires no mask. Consequently, contamination of the catalyst surface through photoresist can be avoided. Furthermore, ink-jet deposition uses the precursor material more efficiently than other techniques since it produces less waste.

In our experiments, an aqueous solution of aluminum chloride ($AlCl_3$) was loaded in a commercial ink-jet printer and deposited onto the copper foil. Medium resolution features can be printed using this approach on large scale samples and Fig. 2a shows a letter sized piece of Cu foil (200 × 270 mm) with aluminum precursor patterns. The maximum graphene size obtained from the patterned Cu-foil is only limited by the dimensions of the CVD chamber, which is 1″ in our experiments. After growth, the patterned graphene could be transferred to other substrates, such as flexible polyethylene terephthalate (PET) (Fig. 2b).

Raman analysis of thus synthesized patterns reveals that the passivation layer efficiently suppresses graphene nucleation as demonstrated by the absence of carbon related Raman features inside the passivated regions (Fig. 2c). We furthermore compare the quality of the patterned graphene to graphene synthesized by traditional CVD methods. For this, the defect related I_D/I_G ratio[18] of 10 000 individual spectra obtained from patterned and pristine graphene was compared (Fig. 2d). The average I_D/I_G ratio of both samples is very similar which confirms that the quality of graphene does not deteriorate through barrier guided growth.

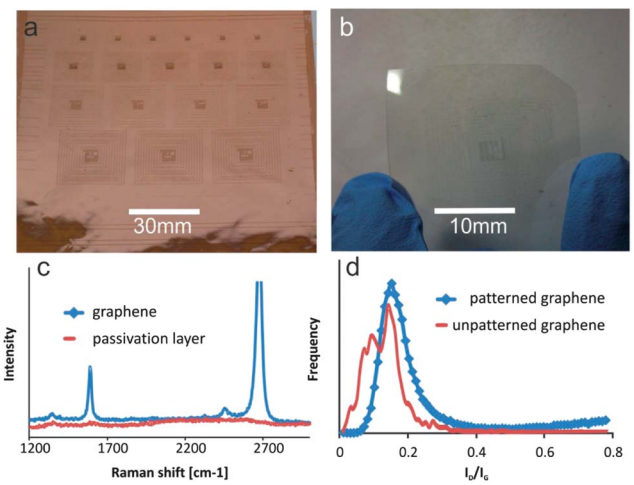

Fig. 2 (a) Patterns deposited by ink-jet printing on copper foil, (b) patterned graphene film after transfer to plastic substrate, (c) Raman spectra of graphene and passivation areas, (d) histograms of I_D/I_G ratio for graphene obtained on patterned substrate and pristine Cu foil.

The absence of conductive pathways and the large band gap of the alumina result in a large resistance (>1 MΩ) of the passivation layer that can be used to isolate graphene areas from one another. This property allows the formation of extended circuits where the passivation layer is used as the dielectric support for active elements and the graphene represents the interconnect layer. The resulting ability to fabricate transparent and flexible circuits is demonstrated in Fig. 2b.

Non-traditional methods readily lend themselves to the deposition of liquid precursors over large areas at high resolution.[19] One such method is the use of microcontact printing which has been used to produce nanometer sized features over square inch scales.[19] Furthermore, the high achievable throughput and long life span of stamps make this technique ideally suitable for large scale production of patterned graphene.

We here use a patterned stamp to deposit parallel strips of nanometer sized Al_2O_3 barriers as shown in Fig. 3. For this, a polydimethylsiloxane (PDMS) replica of a grating with 700 nm pitch was inked with a solution of $AlCl_3$ and then pressed onto Cu-foil.

This presence of large arrays of nanometer-sized Al_2O_3 strips results in a light diffraction effect which confirms the quality of the procedure (Fig. 3a). The thus prepared substrate was subjected to CVD growth and subsequently transferred to a SiO_2 sample. The formation of graphene between the Al_2O_3 strips was first inferred from wrinkles observed by AFM imaging (Fig. 3b). Raman analysis was then conducted to confirm the presence and quality of graphene grown. Similar to the ink-jet printed samples, the graphene quality is comparable to graphene synthesized on pristine Cu foil. Micro-Raman mapping revealed a periodic variation of the intensity of the Raman features as shown in Fig. 3c. The absence of a clear separation between graphene regions and empty barrier regions is due to the similar dimensions of the laser spot size and the graphene feature size. Consequently, a deconvolution of the laser profile has to be performed. Assuming a Gaussian intensity profile of a 1 μm laser spot, we estimate the width of the graphene strips has to be approximately 350 nm to generate the observed Raman line profile. This dimension agrees with AFM measurements of exposed Cu regions with a width of approximately 300 nm.

The high achievable resolution with simple fabrication processes highlights the potential of cheaply and scalably producing nanometer sized graphene structures with resolutions beyond the capabilities of optical lithography. This ability is expected to not only improve the usefulness of graphene interconnects but also enable new applications that can exploit size-dependent effects, *i.e.* quantum dots or nanoribbons for application in opto-electronic devices. The presented approach to generate high quality graphene patterns by different methods that are complementary in resolution and cost will increase the commercial appeal of graphene based devices.

We now demonstrate the potential of the presented approach for the use of graphene in non-planar devices – a novel application of the material. One of graphene's unique properties, brought about by its atomic thickness, is the ability to conform perfectly to rough surfaces. This property could prove useful in fields such as three-dimensional electronics, novel detectors,[20] implantable devices[20] or displays.[4] Conventional lithographical techniques, however, can only produce graphene patterns on flat substrates, due to a limited depth of focus of the optical exposure units, handling issues, *etc.* Thus, non-planar substrates are not accessible for high resolution lithographical patterning. The described direct synthesis technique does not face these limitations since graphene patterning is accomplished on a planar substrate before growth. We here demonstrate that the usually required transfer step that is used to remove the catalytic growth substrate[12] can impart new functionality. Previous reports showed that graphene can be placed onto arbitrary surfaces[12] and we extend this idea by transferring pre-patterned graphene circuits onto complex shaped substrates as demonstrated in Fig. 4.

As a proof of concept, a circuit with 4 clover-leaf-shaped graphene electrodes separated by an Al_2O_3 barrier was produced

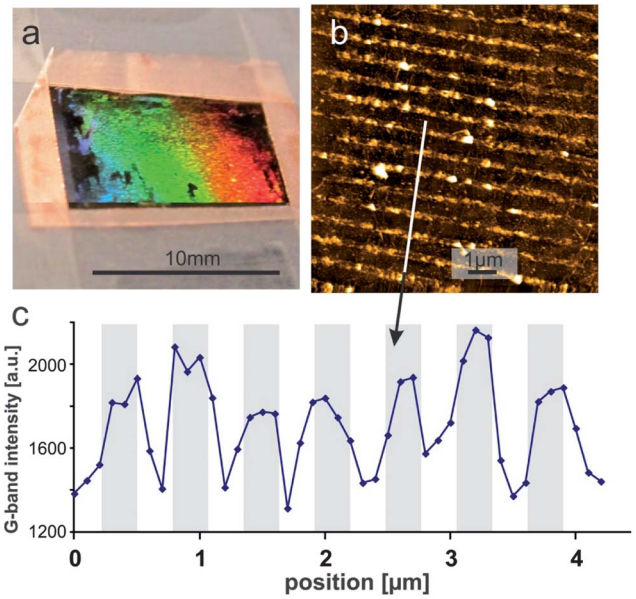

Fig. 3 (a) Photograph of copper foil patterned by microcontact printing deposition of a passivation layer, (b) AFM image of the resulting parallel Al_2O_3 lines with a 700 nm period after growth and transfer (c) variation of G-band intensity across graphene stripes.

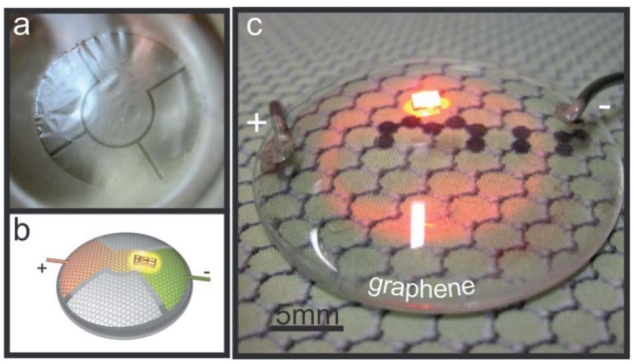

Fig. 4 Transfer of patterned graphene onto complex shaped objects. (a) Photograph of patterned graphene membrane during transfer, (b) schematic of graphene electrode structure, (c) photograph of patterned graphene electrodes on a lens supplying current to a LED.

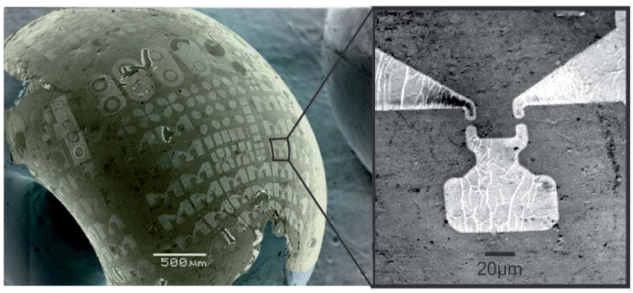

Fig. 5 False-color SEM image of lithographically patterned graphene transferred onto a 3 mm glass torus, (inset) magnification of feature with 5 μm gap feature.

through barrier guided growth. A thin polymer membrane was then deposited onto the patterned graphene to support it during the wet-chemical removal of the Cu substrate (Fig. 4a) shows the floating graphene/polymer membrane. The membrane was then deposited onto a glass lens and the polymer support was removed. This structure can be used as a simple electrical circuit as shown in Fig. 4b where current is directed through the graphene into a light emitting diode that was attached onto the graphene layer (Fig. 4c). This integration of commercially available electronics components into graphene circuits is intended to show their synergy and the potential for more complex circuits.

The described technique is also capable of producing high resolution features on highly complex non-planar substrates. To prove this ability, micrometer resolution patterns were generated on Cu-foil by lithographically preparing a mask on the substrate and blanket deposition of the passivation layer. After growth, the obtained graphene patterns (Fig. 1d) were released from the Cu substrate (Fig. 1e) and transferred onto a 3 millimeter diameter glass toroid. This structure represents one of the most challenging surfaces since it exhibits concave and convex surfaces of different curvatures. After removal of the polymer support, the patterned graphene conforms well to the surface with few imperfections (Fig. 5). Scanning electron microscopy confirms that the generated micrometer sized gaps and channels were still intact after transfer (inset of Fig. 5). Furthermore, the simultaneously transferred Al_2O_3 barrier does not exhibit cracks which is attributed to its low thickness. We therefore envision the fabrication of complete circuits on Cu-substrate and the subsequent transfer onto complex surfaces, which opens up new ways to integrate electronics for a variety of applications, such as implantable devices, bio-inspired circuits, three-dimensional electronics, *etc.*

Conclusions

In conclusion, the scalable and high quality fabrication of graphene patterns using a barrier guided CVD method is reported. Using a solution based approach we produce large area and high resolution passivation features that restrict the graphene growth to certain areas. Several approaches to depositing the patterned passivation layer were demonstrated that are complementary in resolution, scale and cost. Finally, the deposition of pre-patterned graphene onto non-planar substrates was shown and the ability to generate high resolution graphene patterns on complex surfaces opens up novel application areas for electronic devices.

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